Podmiana płyty - File break

(1)

```
sysreset:   revision 5.1 (Mon Apr 27 11:43:53 1992)

 Hit <CR> to continue

iscn68==>load 120d0
pc = 120d0
iscn68==>t
pc=00000000   ipc=040   ep=000   ui=f   head 1
iscn68==>tipr
 80
iscn68==>t
pc=00000000   ipc=080   ep=000   ui=f   head 1
iscn68==>t
pc=00000000   ipc=080   ep=000   ui=f   head 1
iscn68==>t
pc=00000000   ipc=080   ep=000   ui=f   head 1
iscn68==>t
pc=00000000   ipc=080   ep=000   ui=f   head 1
iscn68==>t
pc=00000000   ipc=080   ep=000   ui=f   head 1
iscn68==>t
pc=00000000   ipc=081   ep=000   ui=f   head 1
iscn68==>t
pc=00000000   ipc=068   ep=000   ui=f   head 1
iscn68==>t
pc=00000000   ipc=069   ep=000   ui=f   head 1
iscn68==>t
pc=00000000   ipc=06a   ep=000   ui=f   head 1
iscn68==>t
pc=00000000   ipc=06b   ep=000   ui=f   head 1
iscn68==>t
pc=00000000   ipc=06c   ep=000   ui=f   head 1
iscn68==>t
pc=00000000   ipc=06d   ep=000   ui=f   head 1
iscn68==>t
pc=00000000   ipc=06e   ep=000   ui=f   head 1
iscn68==>t
pc=00000000   ipc=070   ep=000   ui=f   head 1
iscn68==>t
pc=00000000   ipc=071   ep=000   ui=f   head 1
iscn68==>t
pc=000120d0   ipc=c00   ep=000   ui=0   head 1
iscn68==>t
pc=000120d0   ipc=c00   ep=000   ui=0   head 1
iscn68==>t
pc=000120d0   ipc=c00   ep=000   ui=0   head 1
iscn68==>t
pc=000120d0   ipc=011   ep=000   ui=f   head 1
iscn68==>t
pc=000120d0   ipc=110   ep=000   ui=f   head 1
iscn68==>t
pc=000120d0   ipc=111   ep=000   ui=f   head 1
iscn68==>t
pc=000120d0   ipc=111   ep=000   ui=f   head 1
iscn68==>t
pc=000120d0   ipc=112   ep=000   ui=f   head 1
iscn68==>t
pc=000120d0   ipc=112   ep=000   ui=f   head 1
iscn68==>t
pc=000120d0   ipc=112   ep=000   ui=f   head 1
iscn68==>t
pc=000120d0   ipc=129   ep=000   ui=f   head 1
iscn68==>t
pc=000120d0   ipc=12a   ep=000   ui=f   head 1
iscn68==>t
pc=000120d0   ipc=12b   ep=000   ui=f   head 1
iscn68==>t
pc=000120d0   ipc=011   ep=000   ui=0   head 1
iscn68==>t
pc=000120d0   ipc=c00   ep=000   ui=0   head 1
iscn68==>in "fu_mmqueue"

Including: fu_mmqueue


Message: Dump mmqueue with dump_mmq (head #)
 Log_char returning EOF
```

- coldstart complete in pc=120d0
- check Icache =>
- sent PC TO SWAPPER
- => program PTE MISS

↓ Porównując to z debugerem źle
↑ nie dozwolone przejście - wskazuje na uszkodzenie w DC w translatorze adresu log -> fizycz.
i należałoby opróżnić DC
robiliśmy to 2x dla pewności
to samo! tj coldstart i GO 4x

again PTE MISS!
Błąd

zapisuje się
program powrót do tego adresu
w pamięci wirtualnej.

skoro tak to look at

```
iscn68==>dump_mmq                                  and

MMQUEUE        Head  1
NUM                                POP          part  qinh   MOx_EN    MEx_EN   CU
ITEMS  _qpush  empty  full   q  qq  qqq        2    sxv   3 2 1 Ø  3 2 1 Ø  EN
-----  ------  -----  ----   -  --  ---      ----   ---   -------  -------  --
   Ø       1      1      Ø   Ø   Ø   Ø          Ø     1   Ø Ø Ø 1  Ø Ø Ø 1   Ø

o loc   or  bd  gaØ  ga1       req                         full  op       mmq  cu  mxv   inh
k ptr    #  Ø1  <<3  <<3       Ø1*  sz  rot unit   rtn      upd  rdy  vm  act  en  dual  ust
- ----  --  --  ---  -------   ---  --  --- ----   ---      ---  ---  --  ---  --  ----  ---
  wp-> Ø  (next position to be written)
N qw-> Ø  22  ØdØ  cad6aØdØ  11    2    Ø 1  VP    19 S4u     1    1   1    Ø    Ø    1    Ø
N rp-> Ø  22  f8Ø  ØØ3fff8Ø  11    3    Ø 2  IP    Ø8 TØ      1    1   1    Ø    Ø    Ø    Ø

N qr-> Ø  22  f8Ø  ØØ3fff8Ø  11    3    Ø 2  IP    Ø8 TØ      1    1   1    Ø    Ø    Ø    Ø
N      f  22  ff8  ØØ3ffff8  11    3    Ø 2  IP    Ø8 TØ      1    1   1    Ø    Ø    Ø    Ø
N      e  22  ffØ  ØØ3ffffØ  11    3    Ø 2  IP    Ø8 TØ      1    1   1    Ø    Ø    Ø    Ø
N      d  22  fe8  ØØ3fffe8  11    3    Ø 2  IP    Ø8 TØ      1    1   1    Ø    Ø    Ø    Ø
N      c  22  feØ  ØØ3fffeØ  11    3    Ø 2  IP    Ø8 TØ      1    1   1    Ø    Ø    Ø    Ø
N      b  22  fd8  ØØ3fffd8  11    3    Ø 2  IP    Ø8 TØ      1    1   1    Ø    Ø    Ø    Ø
N      a  22  fdØ  ØØ3fffdØ  11    3    Ø 2  IP    Ø8 TØ      1    1   1    Ø    Ø    Ø    Ø
N      9  22  fc8  ØØ3fffc8  11    3    Ø 2  IP    Ø8 TØ      1    1   1    Ø    Ø    Ø    Ø
N      8  22  fcØ  ØØ3fffcØ  11    3    Ø 2  IP    Ø8 TØ      1    1   1    Ø    Ø    Ø
N      7  22  fb8  ØØ3fffb8  11    3    Ø 2  IP    Ø8 TØ      1    1   1    Ø    Ø    Ø    Ø
N      6  22  fbØ  ØØ3fffbØ  11    3    Ø 2  IP    Ø8 TØ      1    1   1    Ø    Ø    Ø    Ø
N      5  22  fa8  ØØ3fffa8  11    3    Ø 2  IP    Ø8 TØ      1    1   1    Ø    Ø    Ø    Ø
N      4  22  faØ  ØØ3fffaØ  11    3    Ø 2  IP    Ø8 TØ      1    1   1    Ø    Ø    Ø    Ø
N      3  22  f98  ØØ3fff98  11    3    Ø 2  IP    Ø8 TØ      1    1   1    Ø    Ø    Ø    Ø
N      2  22  f9Ø  ØØ3fff9Ø  11    3    Ø 2  IP    Ø8 TØ      1    1   1    Ø    Ø    Ø    Ø
N      1  22  f88  ØØ3fff88  11    3    Ø 2  IP    Ø8 TØ      1    1   1    Ø    Ø    Ø    Ø

iscn68==>in "hang"

Including: hang


Display hang state of the cpu with hang (head #)

Default Head [:9ØØ]:

 Log_char returning EOF

iscn68==>hang
         hang                     Cpu  1

IPP:      (pc)       (ba)       (na)         ja  as_pend  vp_pend  inst_rdy
     ØØØ12ØdØ  ØØØØØØØØ  ØØØ12Ød8  ØØØ12ØdØ        Ø        Ø        Ø
              la  la_maxed  pur_state
     ØØØ12ØeØ         Ø          5

ASP: ipc  upc  ui_valid  ui_lvl_1  ip_inh  mem_idle  fu_busy  vc_idle
     cØØ  cØ1       Ø         Ø        Ø         Ø        Ø        1

SFU: vl          vs  vg_busy1  vg_dbusy1  vg_vlc  vg_dvlc  vg_qmop  vg_qsiz
     ØØ  ØØØØØØØØ          Ø          Ø      ff        Ø        Ø        Ø
     mmqempty      vl_rdy_as      vl_rdy_vc     vmq_ptr    vpq_ptr
          1             Ø             Ø            Ø          Ø

DCU: qreq  qfault  qlab_full  qrd_cyc  qwr_cyca  qex_cyc        qla1
       1       Ø          Ø        1         Ø        1     ØØØ12Ød8

VPC: (disp)  ip_disp  (ep)  ul_active_1  ul_uia  ua_active  ua_uia  um_active  um_uia
         Ø        Ø   ØØØ           Ø      ØØØ          Ø     ØØØ          Ø     ØØØ
     lbd_state  dlp_state  os_state_reg  vmo_state_reg
            Ø          Ø             Ø              Ø

iscn68==>dump_mmq

MMQUEUE        Head  1
NUM                                POP          part  qinh   MOx_EN    MEx_EN   CU
ITEMS  _qpush  empty  full   q  qq  qqq        2    sxv   3 2 1 Ø  3 2 1 Ø  EN
-----  ------  -----  ----   -  --  ---      ----   ---   -------  -------  --
   Ø       1      1      Ø   Ø   Ø   Ø          Ø     1   Ø Ø Ø 1  Ø Ø Ø 1   Ø

o loc   or  bd  gaØ  ga1       req                         full  op       mmq  cu  mxv   inh
k ptr    #  Ø1  <<3  <<3       Ø1*  sz  rot unit   rtn      upd  rdy  vm  act  en  dual  ust
```

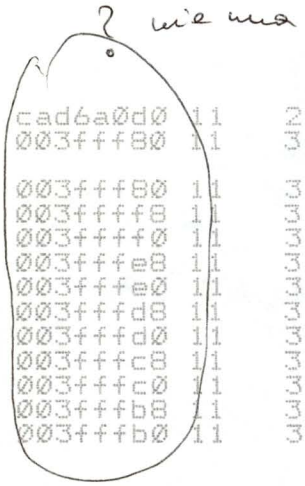
gdzieś tutaj look at dobry wydruk -> tam jest tutaj powien ... się nie jednej z pozycji adres z gLA1

Ale one of these addresses should be in

akurat jest już tutaj next instr. adres

jeden z tych ostatnich powinien być wyżej

wp-> Ø (next position to be written)



N	qw->	Ø	22	Ød Ø	cad6a Ød Ø	11	2	Ø	1	VP	19	S4u	1	1	1	Ø	Ø	1	Ø
N	rp->	Ø	22	f8 Ø	Ø Ø3fff8 Ø	11	3	Ø	2	IP	Ø8	TØ	1	1	1	Ø	Ø	Ø	Ø
N	qr->	Ø	22	f8 Ø	Ø Ø3fff8 Ø	11	3	Ø	2	IP	Ø8	TØ	1	1	1	Ø	Ø	Ø	Ø
N		f	22	ff8	Ø Ø3ffff8	11	3	Ø	2	IP	Ø8	TØ	1	1	1	Ø	Ø	Ø	Ø
N		e	22	ff Ø	Ø Ø3ffff Ø	11	3	Ø	2	IP	Ø8	TØ	1	1	1	Ø	Ø	Ø	Ø
N		d	22	fe8	Ø Ø3fffe8	11	3	Ø	2	IP	Ø8	TØ	1	1	1	Ø	Ø	Ø	Ø
N		c	22	fe Ø	Ø Ø3fffe Ø	11	3	Ø	2	IP	Ø8	TØ	1	1	1	Ø	Ø	Ø	Ø
N		b	22	fd8	Ø Ø3fffd8	11	3	Ø	2	IP	Ø8	TØ	1	1	1	Ø	Ø	Ø	Ø
N		a	22	fd Ø	Ø Ø3fffd Ø	11	3	Ø	2	IP	Ø8	TØ	1	1	1	Ø	Ø	Ø	Ø
N		9	22	fc8	Ø Ø3fffc8	11	3	Ø	2	IP	Ø8	TØ	1	1	1	Ø	Ø	Ø	Ø
N		8	22	fc Ø	Ø Ø3fffc Ø	11	3	Ø	2	IP	Ø8	TØ	1	1	1	Ø	Ø	Ø	
N		7	22	fb8	Ø Ø3fffb8	11	3	Ø	2	IP	Ø8	TØ	1	1	1	Ø	Ø	Ø	Ø
N		6	22	fb Ø	Ø Ø3fffb Ø	11	3	Ø	2	IP	Ø8	TØ	1	1	1	Ø	Ø	Ø	Ø

powiewa w mnqueue nie ma
żadnego z adresów

Uszkodzona płyta FLL w PROCESORZE

test spu4000

```
The current configuration includes the following slots:
  vdb   vcb   dcb   fub   ipb   asb   moØ   meØ   mo1   me1   sp2   cpx   pia   ccu2

[command [slots]] ... (end) :
> remove meo1

The current configuration includes the following slots:
  vdb   vcb   dcb   fub   ipb   asb   moØ   meØ   sp2   cpx   pia   ccu2

[command [slots]] ... (end) :
> remove me1

The current configuration includes the following slots:
  vdb   vcb   dcb   fub   ipb   asb   moØ   meØ   sp2   cpx   pia   ccu2

[command [slots]] ... (end) :
> end

The test configuration includes the following slots:
  vdb   vcb   dcb   fub   ipb   asb   moØ   meØ   sp2   cpx   pia   ccu2

            Subtest 1ØØØ    Ø:ØØ:ØØ   passed
            Subtest 11ØØ    Ø:ØØ:ØØ   passed
            Subtest 12ØØ    Ø:ØØ:Ø2   passed
            Subtest 13ØØ    Ø:ØØ:Ø1   passed
            Subtest 2ØØØ    Ø:ØØ:Ø1   passed
            Subtest 211Ø    Ø:ØØ:Ø1   passed
            Subtest 2111    Ø:ØØ:Ø2   passed
            Subtest 2112    Ø:ØØ:Ø1   passed
            Subtest 2113    Ø:ØØ:Ø1   passed
            Subtest 2114    Ø:ØØ:Ø1   passed
            Subtest 2115    Ø:ØØ:Ø2   passed
            Subtest 22ØØ    Ø:ØØ:Ø1   passed
            Subtest 22Ø2    Ø:ØØ:Ø1   passed
            Subtest 22Ø5    Ø:ØØ:Ø1   passed
            Subtest 22Ø7    Ø:ØØ:Ø2   passed
            Subtest 231Ø    Ø:ØØ:Ø1   passed
            Subtest 2312    Ø:ØØ:ØØ
SPU-OS(1Ø9):Trap: Soft error
  Ø:ØØ:Ø1   passed
            Subtest 234Ø    Ø:ØØ:Ø1   passed
            Subtest 2342    Ø:ØØ:Ø1   passed
            Subtest 2344    Ø:ØØ:Ø1   passed
            Subtest 24Ø2    Ø:ØØ:Ø1   passed
            Subtest 311Ø    Ø:ØØ:Ø4   passed
            Subtest 3111    Ø:ØØ:Ø3   passed
            Subtest 3112    Ø:ØØ:Ø3   passed
            Subtest 3113    Ø:ØØ:Ø3   passed
            Subtest 3114    Ø:ØØ:Ø4   passed
            Subtest 3115    Ø:ØØ:Ø3   passed
            Subtest 32ØØ    Ø:ØØ:Ø3   passed
            Subtest 32Ø5    Ø:ØØ:Ø3   passed
            Subtest 33ØØ    Ø:ØØ:ØØ   passed
            Subtest 331Ø    Ø:ØØ:Ø3   passed
            Subtest 334Ø    Ø:ØØ:Ø4   passed
            Subtest 34Ø2    Ø:ØØ:Ø3   passed
            Subtest 411Ø    Ø:ØØ:Ø1   passed
            Subtest 4111    Ø:ØØ:Ø1   passed
            Subtest 4112    Ø:ØØ:Ø1   passed
            Subtest 4113    Ø:ØØ:Ø1   passed
            Subtest 4114    Ø:ØØ:Ø2   passed
            Subtest 4115    Ø:ØØ:Ø1   passed
            Subtest 4116    Ø:ØØ:Ø2   passed
            Subtest 42ØØ    Ø:ØØ:Ø1   passed
            Subtest 42Ø2    Ø:ØØ:Ø2   passed
            Subtest 42Ø5    Ø:ØØ:Ø1   passed
            Subtest 42Ø7    Ø:ØØ:Ø2   passed
            Subtest 431Ø    Ø:ØØ:Ø1   passed
            Subtest 4312    Ø:ØØ:Ø2   passed
            Subtest 434Ø    Ø:ØØ:13   failed

*****   Thu Feb 11 12:30:14 1993   *****
Test:    spu4ØØØ.t  1.18   Class: 4     Subtest: 434Ø 1.13 Count: 1     Error:
Failed:  PIA Scan Ring Integrity

scan ring failure in bidirection part of scan ring isolated
failing bit (Ø - Øx17f (Ø - 383)): Øxd4 (212)
failure detected when writing and reading in the LEFT direction
isolation done by writing LEFT, reading RIGHT
```

VDB
VCB
Mx1
ME1

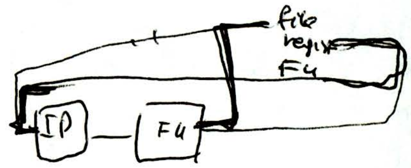
talks to all board in computer
failed on subtest 4320
so mminit presredt bo
ou idzie po 2BUSIE
coldstart to SCAN BASIE.

```
expected buffer:
Øxd6 (214) bits in buffer - Øx6 (6) bits in MSW - LSB is lower right bit
                  Øx001f  Øxffff  Øxffff  Øxffff  Øxffff  Øxffff
  Øxffff  Øxffff  Øxffff  Øxffff  Øxffff  Øxffff  Øxffff  Øxffff

actual buffer:
Øxd6 (214) bits in buffer - Øx6 (6) bits in MSW - LSB is lower right bit
                  Øx000f  Øxffff  Øxffff  Øxffff  Øxffff  Øxffff
  Øxffff  Øxffff  Øxffff  Øxffff  Øxffff  Øxffff  Øxffff  Øxffff

Test 'spu4000.t' failed
Elapsed time:   0:01:37
: spu4000
$$$     error in process diagnostic shell
$$$     illegal command 'spu4000'
: test spu4000
spu4000.t:   unable to deterermine software revision

Test 'spu4000.t'                          Thu Feb 11 12:32:09 1993


The current configuration includes the following slots:
  vdb  vcb  dcb  fub  ipb  asb  mo0  me0  mo1  me1  sp2  cpx  pia  ccu2

[command [slots]] ... (end) :
> remove all

The current configuration includes the following slots:

[command [slots]] ... (end) :
> add vdb vcb mo1 me1

The current configuration includes the following slots:
  vdb  vcb  mo1  me1

[command [slots]] ... (end) :
> end

The test configuration includes the following slots:
  vdb  vcb  mo1  me1

        Subtest 2114    0:00:01   passed
        Subtest 2115    0:00:01   passed
        Subtest 2210    0:00:01   passed
        Subtest 2212    0:00:01   passed
        Subtest 2215    0:00:01   passed
        Subtest 2217    0:00:01   passed
        Subtest 3114    0:00:03   passed
        Subtest 3115    0:00:03   passed
        Subtest 3210    0:00:03   passed
        Subtest 3215    0:00:03   passed
        Subtest 4114    0:00:02   passed
        Subtest 4115    0:00:01   passed
        Subtest 4116    0:00:02   passed
        Subtest 4210    0:00:01   passed
        Subtest 4212    0:00:01   passed
        Subtest 4215    0:00:01   passed
        Subtest 4217    0:00:01   passed
        Subtest 5114    0:00:02   passed
        Subtest 5115    0:00:02   passed
        Subtest 5210    0:00:02   passed
        Subtest 5215    0:00:03   passed
        Subtest 6114    0:00:02   passed
        Subtest 6210    0:00:02   passed
        Subtest 6215    0:00:02   passed

Test 'spu4000.t' passed
Elapsed time:   0:00:48
: test spu4000
spu4000.t:   unable to deterermine software revision

Test 'spu4000.t'                          Thu Feb 11 12:34:39 1993


The current configuration includes the following slots:
  vdb  vcb  dcb  fub  ipb  asb  mo0  me0  mo1  me1  sp2  cpx  pia  ccu2

[command [slots]] ... (end) :
> remove all
```

```
The current configuration includes the following slots:

[command [slots]] ... (end) :
> add moØ meØ

The current configuration includes the following slots:
  moØ  meØ

[command [slots]] ... (end) :
> end

The test configuration includes the following slots:
  moØ  meØ

        Subtest 22ØØ    Ø:ØØ:Ø2   passed
        Subtest 22Ø2    Ø:ØØ:Ø1   passed
        Subtest 22Ø5    Ø:ØØ:Ø1   passed
        Subtest 22Ø7    Ø:ØØ:Ø1   passed
        Subtest 32ØØ    Ø:ØØ:Ø3   passed
        Subtest 32Ø5    Ø:ØØ:Ø3   passed
        Subtest 42ØØ    Ø:ØØ:Ø2   passed
        Subtest 42Ø2    Ø:ØØ:Ø1   passed
        Subtest 42Ø5    Ø:ØØ:Ø2   passed
        Subtest 42Ø7    Ø:ØØ:Ø1   passed
        Subtest 52ØØ    Ø:ØØ:Ø3   passed
        Subtest 52Ø5    Ø:ØØ:Ø2   passed
        Subtest 62ØØ    Ø:ØØ:Ø2   passed
        Subtest 62Ø5    Ø:ØØ:Ø2   passed
```

ok memory

```
Test 'spu4ØØØ.t' passed
Elapsed time:   Ø:ØØ:27
:
: test spu4ØØØ
spu4ØØØ.t:   unable to deterermine software revision

Test 'spu4ØØØ.t'                        Thu Feb 11 12:4Ø:29 1993

The current configuration includes the following slots:
  vdb  vcb  dcb  fub  ipb  asb  moØ  meØ  mo1  me1  sp2  cpx  pia  ccu2

[command [slots]] ... (end) :
> remove all

The current configuration includes the following slots:

[command [slots]] ... (end) :
> add pia

The current configuration includes the following slots:
  pia

[command [slots]] ... (end) :
> end

The test configuration includes the following slots:
  pia

        Subtest 234Ø    Ø:ØØ:Ø1   passed
        Subtest 2342    Ø:ØØ:Ø1   passed
        Subtest 2344    Ø:ØØ:Ø1   passed
        Subtest 334Ø    Ø:ØØ:Ø4   passed
        Subtest 434Ø    Ø:ØØ:13   failed
```



podtesty preszły; Vector procesor i Memory itd idą po tej samej szynie. u nas więc wykonała się operacja multiply (wcześniej urwany wydruk. One idą po SCAN BASIE a wyniki operacji skoncl. mnożenie po 2 BUSIE. WYNIKA Z POPRZEDNIEGO POST. SKORO ALL TESTY PRZESZŁY TO PIA o BAB

```
*****  Thu Feb 11 12:41:31 1993  *****
Test:      spu4ØØØ.t   1.18   Class: 4    Subtest: 434Ø 1.13 Count: 1     Error:
Failed:    PIA Scan Ring Integrity

scan ring failure in bidirection part of scan ring isolated
failing bit (Ø - Øx17f (Ø - 383)): Øxd4 (212)
failure detected when writing and reading in the LEFT direction
isolation done by writing LEFT, reading RIGHT

expected buffer:
Øxd6 (214) bits in buffer - Øx6 (6) bits in MSW - LSB is lower right bit
                        ØxØØ1f  Øxffff  Øxffff  Øxffff  Øxffff  Øxffff
  Øxffff  Øxffff  Øxffff  Øxffff  Øxffff  Øxffff  Øxffff  Øxffff

actual buffer:
```

```
Øxd6 (214) bits in buffer - Øx6 (6) bits in MSW - LSB is lower right bit



                    Øx000f  Øxffff  Øxffff  Øxffff  Øxffff  Øxffff
  Øxffff  Øxffff  Øxffff  Øxffff  Øxffff  Øxffff  Øxffff  Øxffff

Test 'spu4000.t' failed
Elapsed time:    Ø:ØØ:23
: test spu4000
spu4000.t:   unable to deterermine software revision

Test 'spu4000.t'                              Thu Feb 11 12:43:37 1993


The current configuration includes the following slots:
  vdb  vcb  dcb  fub  ipb  asb  moØ  meØ  mo1  me1  sp2  cpx  pia  ccu2

[command [slots]] ... (end) :
> remove pia

The current configuration includes the following slots:
  vdb  vcb  dcb  fub  ipb  asb  moØ  meØ  mo1  me1  sp2  cpx  ccu2

[command [slots]] ... (end) :
> end

The test configuration includes the following slots:
  vdb  vcb  dcb  fub  ipb  asb  moØ  meØ  mo1  me1  sp2  cpx  ccu2

        Subtest 1ØØØ    Ø:ØØ:ØØ   passed
        Subtest 11ØØ    Ø:ØØ:ØØ   passed
        Subtest 12ØØ    Ø:ØØ:Ø2   passed
        Subtest 13ØØ    Ø:ØØ:Ø1   passed
        Subtest 2ØØØ    Ø:ØØ:Ø1   passed
        Subtest 211Ø    Ø:ØØ:Ø1   passed
        Subtest 2111    Ø:ØØ:Ø1   passed
        Subtest 2112    Ø:ØØ:Ø1   passed
        Subtest 2113    Ø:ØØ:Ø1   failed

*****  Thu Feb 11 12:43:59 1993  *****
Test:    spu4ØØØ.t  1.18   Class: 2    Subtest: 2113 1.13 Count: 1    Error:
Failed:  DCB Scan I/F
MSB failure:    wrote 1, read Ø

Test 'spu4000.t' failed
Elapsed time:    Ø:ØØ:11
: !sysreset
sysreset:    revision 5.1 (Mon Apr 27 11:43:53 1992)
: test spu4000
spu4000.t:   unable to deterermine software revision

Test 'spu4000.t'                              Thu Feb 11 12:44:5Ø 1993


The current configuration includes the following slots:
  vdb  vcb  dcb  fub  ipb  asb  moØ  meØ  mo1  me1  sp2  cpx  pia  ccu2

[command [slots]] ... (end) :
> remove pia

The current configuration includes the following slots:
  vdb  vcb  dcb  fub  ipb  asb  moØ  meØ  mo1  me1  sp2  cpx  ccu2

[command [slots]] ... (end) :
> end

The test configuration includes the following slots:
  vdb  vcb  dcb  fub  ipb  asb  moØ  meØ  mo1  me1  sp2  cpx  ccu2

        Subtest 1ØØØ    Ø:ØØ:ØØ   passed
        Subtest 11ØØ    Ø:ØØ:ØØ   passed
        Subtest 12ØØ    Ø:ØØ:Ø3   passed
        Subtest 13ØØ    Ø:ØØ:Ø1   passed
        Subtest 2ØØØ    Ø:ØØ:ØØ   passed
        Subtest 211Ø    Ø:ØØ:Ø2   passed
        Subtest 2111    Ø:ØØ:Ø1   passed
        Subtest 2112    Ø:ØØ:Ø1   passed
        Subtest 2113    Ø:ØØ:Ø1   passed
        Subtest 2114    Ø:ØØ:Ø1   passed
        Subtest 2115    Ø:ØØ:Ø1   passed
        Subtest 22ØØ    Ø:ØØ:Ø1   passed
        Subtest 22Ø2    Ø:ØØ:Ø1   passed
```

SPU Talk to all boards so something is no BIA, SCAN BUS OK BO PODRZEDNIE

```
Subtest 2205     0:00:01     passed




Subtest 2207     0:00:01     passed
Subtest 2210     0:00:01     passed
Subtest 2212     0:00:01     passed
Subtest 2215     0:00:01     passed
Subtest 2217     0:00:01     passed
Subtest 2310     0:00:01     passed
Subtest 2312     0:00:01     passed
Subtest 2402     0:00:01     passed
Subtest 3110     0:00:04     passed
Subtest 3111     0:00:03     passed
Subtest 3112     0:00:03     passed
Subtest 3113     0:00:03     passed
Subtest 3114     0:00:04     passed
Subtest 3115     0:00:03     passed
Subtest 3200     0:00:03     passed
Subtest 3205     0:00:03     passed
Subtest 3210     0:00:03     passed
Subtest 3215     0:00:03     passed
Subtest 3300     0:00:01     passed
Subtest 3310     0:00:03     passed
Subtest 3402     0:00:04     passed
Subtest 4110     0:00:01     passed
Subtest 4111     0:00:01     passed
Subtest 4112     0:00:01     passed
Subtest 4113     0:00:01     passed
Subtest 4114     0:00:01     passed
Subtest 4115     0:00:02     passed
Subtest 4116     0:00:01     passed
Subtest 4200     0:00:02     passed
Subtest 4202     0:00:01     passed
Subtest 4205     0:00:02     passed
Subtest 4207     0:00:01     passed
Subtest 4210     0:00:02     passed
Subtest 4212     0:00:01     passed
Subtest 4215     0:00:02     passed
Subtest 4217     0:00:01     passed
Subtest 4310     0:00:02     passed
Subtest 4312     0:00:01     passed
Subtest 4402     0:00:02     passed
Subtest 5110     0:00:02     passed
Subtest 5111     0:00:02     passed
Subtest 5112     0:00:00     not executed     board is not a cxm
Subtest 5113     0:00:02     passed
Subtest 5114     0:00:02     passed
Subtest 5115     0:00:02     passed
Subtest 5200     0:00:02     passed
Subtest 5205     0:00:03     passed
Subtest 5210     0:00:02     passed
Subtest 5215     0:00:03     passed
Subtest 5310     0:00:02     passed
Subtest 6114     0:00:02     passed
Subtest 6200     0:00:02     passed
Subtest 6205     0:00:02     passed
Subtest 6210     0:00:02     passed
Subtest 6215     0:00:02     passed
Subtest 6310     0:00:03     passed
Subtest 7000     0:00:03     passed
Subtest 7010     0:00:55     passed
Subtest 7100     0:00:53     passed   ← Widać, że wyrzucają PIA all przeszły
Subtest 7110     0:00:02     passed
Subtest 7200     0:00:00     failed   ← tutaj błąd bo sprawdza lock opis wszystkie kwer mind

*****  Thu Feb 11 12:49:05 1993  *****
Test:    spu4000.t  1.18   Class: 7    Subtest: 7200 1.5   Count: 1     Error:
Failed:  EBUS Transfer
ebus operation caused segmentation violation
window map address: 0x00ffa000   window map data: 0x10000000
actual BSR: 0xff10

Test 'spu4000.t' failed
Elapsed time:    0:04:07
: q
p(spu) > wrdwn
pwrdwn: Ready for power down. ^D to abort z?????????????????????????????????????
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```

(1) FU.

```
                CONVEX DIAGNOSTIC TEST MENU
Dir.        Test                Rev.    Description
_____       _________________   _____   _______________

/mnt/test
            cpu4010.t           1.15    C2XX Referenced and Modified Bit Test
            cpu4030.t           1.30    C2XX CPU FUNCTIONAL DIAGNOSTICS
            cpu4040.t           1.13    VECTOR CONCURRENCY TESTS
            cpu4041.t           1.30    C2XX CPU FUNCTIONAL DIAGNOSTICS
            cpu4231.t           1.30    C2XX CPU FUNCTIONAL DIAGNOSTICS
            cpu4232.t           1.30    C2XX CPU FUNCTIONAL DIAGNOSTICS
            cpu4233.t           1.30    C2XX CPU FUNCTIONAL DIAGNOSTICS
            cpu4241.t           1.30    C2XX CPU FUNCTIONAL DIAGNOSTICS
            cpu4XXX.t           1.30    C2XX CPU FUNCTIONAL DIAGNOSTICS
            cpx4000.t           1.13    CPX/CUE,COU Utility board test
            dev4100.t           1.36    Xylogics 450/451 Controller Test Program
            dev4110.t           1.36    Xylogics 450/451 Controller Test Program
            dev4200.t           1.21    STC Tape Drive Test Program
            dev4300.t           1.24    Systech Comm Test Program
            dev4400.t           1.18    MLP2000 Controller, Line Printer Diagnostic
            dev4410.t           1.7     IKON Controller, Versatec Plotter Diagnostic

Page 1 - Enter <CR>, b, p, q, t, or ? for details: q
: test cpu4231
cpu4231.t:   unable to deterermine software revision

Test 'cpu4231.t'                              Wed Feb 10 15:26:40 1993


                        ENTER TEST PARAMETERS

          []        Encloses allowed input ranges or values
          ()        Encloses the default value
          ^         Returns to the previous prompt
          :nn       Returns to the prompt # nn
          :         Returns to the first unsatisfied prompt
          :?        Reviews previous entries

 1: Run default switches? [y,n]                          (y) ->

                    TEST PARAMETER SUMMARY

Run default switches?                                        : y

Loading and initializing test ...  0:02:49
          Current Memory Allocation
File No.  Physical  Address Pid File Name                    Logical Offset
       1  00200000-00226fff   0 p0r0_4231                   00000000
       2  00227000-00ffffff   0 cpu4231.rnn                 0002d000
          10000000-1069ffff   0 cpu4231.rnn                 (cont)
       3  106a0000-106a8fff   0 support_4231                9fffd000
       4  106a9000-106bbfff   0 p0rN_4231                   20000000
       5  106bc000-106cefff   0 p0rN_4231                   40000000
       6  106cf000-106e1fff   0 p0rN_4231                   60000000
       7  106e2000-106f4fff   0 p0rN_4231                   80000000
       8  106f5000-106fafff   0 segment7                    e0000000
       9  106fb000-10702fff   0 st_323_spt                  f0fff000
    -----  23ef0000-23ef1fff   0 pte2                       NA
    -----  23ef2400-23ef2fff   0 ptet                       NA
    -----  23ef3000-23efafff   0 pte2                       NA
    -----  23efb200-23efb7ff   0 pte1                       NA
    -----  23efb800-23ffbfff   0 ptet                       NA
    -----  23ffc000-23ffcfff   0 pte2                       NA
    -----  23ffd000-23ffdfff   0 ptet                       NA
    -----  23ffe000-23ffefff   0 pte2                       NA
    -----  23fff000-23fff5ff   0 pte1                       NA
    -----  23fff600-23fffdff   0 ptet                       NA
    -----  23fffe00-23ffffff   0 pte1                       NA
          Subtest   10     0:00:01    failed

*****  Wed Feb 10 15:29:37 1993  *****
```

```
Test:     cpu4231.t   1.30    Class: 1     Subtest: 10 1.25    Count: 1     Error: 
```

```
Failed:  System calls
HARD ERROR DETECTED
hard_logger:    revision 5.1 (Mon Apr 27 11:43:51 1992)
ME0/MCM: hard_err is not set
ME0/MCM: soft_err is not set
MO0/MCM: hard_err is not set
MO0/MCM: soft_err is not set
ME1/MCM: hard_err is not set
ME1/MCM: soft_err is not set
MO1/MCM: hard_err is not set
MO1/MCM: soft_err is not set
CPX: hard_err is not set
CPX: soft_errs is not set
CPX: hard_err is not set
CPX: soft_errs is not set
PIA: hard_err is not set
PIA: softerr is not set
ASB/ASP: hard_err is not set
DCB/DCU: hard_err is not set
IPB/IPP: Hard error detected.
IPB/IPP: [#303] icache_par_err = 1532
IPB/IPP: l.inst_0 msh bad.
IPB/IPP: l.inst_1 msh bad.
IPB/IPP: l.inst_2 msh bad.
IPB/IPP: l.inst_3 lsh bad.
IPB/IPP: l.icache_tag<31..24> bad.
IPB/IPP: l.siz_0 etc. bad.
IPB/IPP: [#304] la_par_err = 7
IPB/IPP: l.la_tag<31..24> bad.
IPB/IPP: l.la_tag<23..16> bad.
IPB/IPP: l.la_tag<15..13> bad.

VCB/VPC: hard_err is not set
VCB/VPC: softerr is not set
VDB/VPD: hard_err is not set

Register dump for cpu: 1
a0: 00000000  s0: 00000000 00000000  t0: 00000000   pc:  00000000
a1: 00000000  s1: 00000000 00000000  t1: 0002e000  psw:  000000d0
a2: 00000000  s2: 00000000 00000000  t2: 00000000  ipc:       04e
a3: 00000000  s3: 00000000 00000000  t3: 00000000  ccr:    680000
a4: 00000000  s4: 00000000 00000000  t4: 0000001b  cir:    0  tid: 00
a5: 00000000  s5: 00000000 00000000  t5: 0002e000   vl:  00   vs: 00000000
a6: 00000000  s6: 00000000 00000000  t6: 0ad6bad7 vm_u:  00000000 00000000
a7: 00000000  s7: 00000000 00000000  t7: 00000000 vm_l:  00000000 00000000
global_int_enab: 00  local_int_enab: ff  int_mode: 00  target_CPU: 0  ION: 0

Test 'cpu4231.t' failed
Elapsed time:    0:00:31
: q
Hit any character to continue('q' to stop):

 Hit &lt;CR&gt; to continue

iscn68==>q
(spu)> pwrdwn
pwrdwn: Ready for power down. ^D to abort z??????????????????????????????????
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123456789ABCDE

Convex Front Panel / Module Rev: 1.14, Version: 1 Class: 2 / CPU SN 8211
mode-of-operation = normal-os              boot-device = disk
location-of-bootstrap = default            power-up-reboot = enable
automatic-reboot = enable                  spu-selftest = enable
```

look in handout for #303

sugeruje że coś z IPP

os_flags = 0 remote-port-bps = 1200

START

(fp)> boot

```
Waiting for disk ready.
SPU OS version 6.1.0.0
available memory = 909312 (888 Kbytes)
SPU root file system check in progress...
/dev/dk0b: 156 files 1760 blocks 2198 free
SPU mounted file systems check in progress...
/dev/rdk0f: 5 files 8 blocks 11095 free
/dev/rdk0e: 316 files 5576 blocks 35010 free
/dev/rdk0d: 561 files 38831 blocks 42343 free
SPU file system verified
Mounted /mnt on /dev/dk0d
Mounted /hw on /dev/dk0e
Mounted /tmp on /dev/dk0f
SPU OS booted Feb 10 16:07 1993 after power up.  Freq: 60 Hz.
Wed Feb 10 16:12:04 CST 1993

Using cop to determine installed boards ...
Using scnlink to initialize scan structures ...
scnlink:    revision 5.1 (Mon Apr 27 11:43:53 1992)
Using reset_cpus to reset cpu scanability ...
reset_cpus:    revision 5.1 (Mon Apr 27 11:43:53 1992)
sysreset:    revision 5.1 (Mon Apr 27 11:43:53 1992)
sysreset:    revision 5.1 (Mon Apr 27 11:43:53 1992)
sysreset:    revision 5.1 (Mon Apr 27 11:43:53 1992)
sysreset:    revision 5.1 (Mon Apr 27 11:43:53 1992)
Using mcm3_config to determine memory configuration ...
mcm3_config:    revision 5.1 (Mon Apr 27 11:43:52 1992)
mcm3_config:    memory configuration:
    #    type    config
    0    mcm
    1    mcm
    2    mcm
    3    mcm
config_chk:    revision 5.1 (Mon Apr 27 11:43:51 1992)
config_chk:    processor configuration:
    Processor Type: C32XX     Machine Class: 2    Serial Number: 8211
    CPU              0    1
    installed:            X
    available:            X
Initializing system config files
sysreset:    revision 5.1 (Mon Apr 27 11:43:53 1992)

SPU-OS(108):Trap: Hard error
mminit:    revision 5.1 (Mon Apr 27 11:43:52 1992)
mminit:    generating PCM
mminit:    initializing PI, CU, and SP PCMs:    0:00:10

Main memory size:  100663296 bytes - 98304 K - 96 Meg

pair  allocated 16 meg PCM blocks, from a system perspective
 0       0  16
 1      64  65  66  67
 2
 3


+++>
<Wed Feb 10 16:14:55 1993>   mminit:../pcm.c:725
SW Warning (DiagWN196): mismatched memory pairs

memory pairs 0 and 1 are not populated identically
using 8 way interleave
****
mminit:    interleave set to 8-way
Initialization completed.


Booting ConvexOS.  Type ^C to abort
System Initialization
config_chk:    revision 5.1 (Mon Apr 27 11:43:51 1992)
config_chk:    processor configuration:
    Processor Type: C32XX     Machine Class: 2    Serial Number: 8211
    CPU              0    1
    installed:            X
    available:            X
sysreset:    revision 5.1 (Mon Apr 27 11:43:53 1992)
margin:    revision 5.1 (Mon Apr 27 11:43:52 1992)
```

Margin conditions

```
              clk: n +25.01 MHZ
               +5: n  +5.1  VDC
              +12: n +12.1  VDC
               -5: n  -5.2  VDC
              -12: n -12.3  VDC
               -2: n  -2.0  VDC
             -4.5: n  -4.5  VDC

Loading control stores
Opened file /mnt/usr/ucode/us.200.wcs  Rev 11.10
Opened file /mnt/usr/ucode/sr.wcs  Rev 11.4
Opened file /mnt/usr/ucode/ua.wcs  Rev 10.10
Opened file /mnt/usr/ucode/ul.wcs  Rev 10.3
Opened file /mnt/usr/ucode/um.wcs  Rev 10.6
Opened file /mnt/usr/ucode/vd.200.wcs  Rev 10.1
Loading Scalar Control Store: us                    0:23
Verifying Scalar Control Store: us                  0:17
Loading Scalar Control Store: sr                    0:26
Verifying Scalar Control Store: sr                  0:28
Loading Vector Control Stores: ua ul um vd                0:06
Verifying Vector Control Stores: ua ul um vd              0:08

sysreset:   revision 5.1 (Mon Apr 27 11:43:53 1992)
sysreset:   revision 5.1 (Mon Apr 27 11:43:53 1992)
mminit:   revision 5.1 (Mon Apr 27 11:43:52 1992)
mminit:   using PCM from /mnt/boot_db
mminit:   initializing PI, CU, and SP PCMs:   0:00:10

Main memory size:  100663296 bytes - 98304 K - 96 Meg

pair  allocated 16 meg PCM blocks, from a system perspective
 0       0   16
 1      64   65   66   67
 2
 3


+++>
<Wed Feb 10 16:18:22 1993>   mminit:../pcm.c:725
SW Warning (DiagWN196): mismatched memory pairs

memory pairs 0 and 1 are not populated identically
using 8 way interleave
****
mminit:   interleave set to 8-way
mminit:   using CPU 1 to initialize memory:   0:00:05
+++>
<Wed Feb 10 16:18:33 1993>   mminit:../errlog.c:104
SW Error (DiagER217): cpurequest () failed

mminit:   error:   hard error occurred

****
hard_logger:   revision 5.1 (Mon Apr 27 11:43:51 1992)
ME0/MCM: hard_err is not set
ME0/MCM: Soft errors disabled.
ME0/MCM: soft_err is not set
MO0/MCM: hard_err is not set
MO0/MCM: Soft errors disabled.
MO0/MCM: soft_err is not set
ME1/MCM: hard_err is not set
ME1/MCM: Soft errors disabled.
ME1/MCM: soft_err is not set
MO1/MCM: hard_err is not set
MO1/MCM: Soft errors disabled.
MO1/MCM: soft_err is not set
CPX: hard_err is not set
CPX: soft_errs is not set
CPX: hard_err is not set
CPX: soft_errs is not set
PIA: hard_err is not set
PIA: softerr is not set
ASB/ASP: hard_err is not set
DCB/DCU: Hard error detected.
DCB/DCU: [#202] Data Cache Tag parity error
DCB/DCU: [#203] Parity error in remote validate RAMs:
DCB/DCU: Port B, Side 0          Bits <23..16>
DCB/DCU: Port B, Side 1          Bits <23..16>
DCB/DCU: Port E, Side 0          Bits <23..16>
```

CPU1 nie może zainicjować memory.

! ERROR sugeruje zł OC Board

```
DCB/DCU: Port E, Side 1          Bits <23..16>




IPB/IPP: hard_err is not set
VCB/VPC: hard_err is not set
VCB/VPC: softerr is not set
VDB/VPD: hard_err is not set
  0:00:27

+++>
<Wed Feb 10 16:18:52 1993>   mminit:../mminit.c:654
SW Error (DiagER210): mminit failed

mminit:   initialization by CPU 1 failed

****
Initialization Aborted
(spu)> (spu)> cpureg

Register dump for cpu: 1
a0: ffffff00  s0: ffffffff ffffffff  t0: 00000000   pc:  00000000
a1: dfffb7ff  s1: ffffffff ffffffff  t1: 00001014  psw:  666f0950
a2: ffffffff  s2: ffffffff ffffffff  t2: 00000000  ipc:      04e
a3: ffffffff  s3: ffffffff ffffffff  t3: ffffffff  ccr:   680000
a4: ffffffc8  s4: ffffffff ffffffff  t4: 00000001  cir:    0  tid: 00
a5: ffffffff  s5: ffffffff ffffffff  t5: 00001014   vl:  00   vs: 00000000
a6: ffffffff  s6: ffffffff ffffffff  t6: 0ad6bad7 vm_u:  00000000 00000000
a7: ffffffff  s7: ffffffff ffffffff  t7: 0ad4bad5 vm_l:  00000000 00000000
global_int_enab: 00  local_int_enab: ff  int_mode: 00  target_CPU: 0  ION: 0
(spu)> cpureg -i 0

Register dump for cpu: 1
a0: 00000000  s0: 00000000 00000000  t0: 00000000   pc:  00000000
a1: 00000000  s1: 00000000 00000000  t1: 00000000  psw:  666f0950
a2: 00000000  s2: 00000000 00000000  t2: 00000000  ipc:      04e
a3: 00000000  s3: 00000000 00000000  t3: 00000000  ccr:   680000
a4: 00000000  s4: 00000000 00000000  t4: 00000000  cir:    0  tid: 00
a5: 00000000  s5: 00000000 00000000  t5: 00000000   vl:  00   vs: 00000000
a6: 00000000  s6: 00000000 00000000  t6: 00000000 vm_u:  00000000 00000000
a7: 00000000  s7: 00000000 00000000  t7: 00000000 vm_l:  00000000 00000000
global_int_enab: 00  local_int_enab: ff  int_mode: 00  target_CPU: 0  ION: 0
(spu)> sysreset
sysreset:   revision 5.1 (Mon Apr 27 11:43:53 1992)
(spu)> sysreset -l2
sysreset:   revision 5.1 (Mon Apr 27 11:43:53 1992)
(spu)> dshell


CONVEX DIAGNOSTIC SHELL

: test cpu4030
cpu4030.t:   unable to deterermine software revision

Test 'cpu4030.t'                          Wed Feb 10 16:22:15 1993


                    ENTER TEST PARAMETERS

        []      Encloses allowed input ranges or values
        ()      Encloses the default value
        ^       Returns to the previous prompt
        :nn     Returns to the prompt # nn
        :       Returns to the first unsatisfied prompt
        :?      Reviews previous entries

 1: Run default switches? [y,n]                    (y) ->

                  TEST PARAMETER SUMMARY

Run default switches?                                  : y

Loading and initializing test ...  0:00:28
        Current Memory Allocation
File No. Physical  Address Pid File Name                  Logical Offset
       1  00200000-00207fff   0 p0r0_4030                 00000000
       2  00208000-0023bfff   0 cpu4030.rnn               00012000
       3  0023c000-0023dfff   0 p0rN_4030                 20000000
       4  0023e000-0023ffff   0 p0rN_4030                 40000000
       5  00240000-00241fff   0 p0rN_4030                 60000000
       6  00242000-00243fff   0 p0rN_4030                 80000000
```

jeszcze dobrze bo abort boot ← so coldstart nie wykonał się oficjalnie

```
       7   00244000-00246fff    0 pccarry_4030                0000f000

       8   00247000-00249fff    0 pccarry_4030                000ff000
       9   0024a000-0024cfff    0 pccarry_4030                00fff000
      10   0024d000-0024ffff    0 pccarry_4030                0ffff000
      11   00250000-00250fff    0 wrapu_4030                  1ffff000
      12   00251000-00251fff    0 wrapu_4030                  3ffff000
      13   00252000-00252fff    0 wrapu_4030                  5ffff000
      14   00253000-00253fff    0 wrapu_4030                  7ffff000
      15   00254000-00254fff    0 wrapu_4030                  9ffff000
      16   00255000-00255fff    0 wrapu_4030                  bffff000
      17   00256000-00256fff    0 wrapu_4030                  dffff000
      18   00257000-00257fff    0 wrapu_4030                  fffff000
      19   00258000-00258fff    0 wrapl_4030                  a0000000
      20   00259000-00259fff    0 wrapl_4030                  c0000000
      21   0025a000-0025afff    0 wrapl_4030                  e0000000
    -----  23feb000-23ffefff    0 pte2                        NA
    -----  23fff000-23ffffff    0 pte1                        NA
         Subtest   1    0:00:01   failed

*****  Wed Feb 10 16:22:53 1993  *****
Test:    cpu4030.t  1.30   Class: 1    Subtest: 1  1.25    Count: 1    Error: 0
Failed:  ld.h/w #N,ak
HARD ERROR DETECTED
hard_logger:   revision 5.1 (Mon Apr 27 11:43:51 1992)
ME0/MCM: hard_err is not set
ME0/MCM: soft_err is not set
MO0/MCM: hard_err is not set
MO0/MCM: soft_err is not set
ME1/MCM: hard_err is not set
ME1/MCM: soft_err is not set
MO1/MCM: hard_err is not set
MO1/MCM: soft_err is not set
CPX: hard_err is not set
CPX: soft_errs is not set
CPX: hard_err is not set
CPX: soft_errs is not set
PIA: hard_err is not set
PIA: softerr is not set
ASB/ASP: hard_err is not set
DCB/DCU: Hard error detected.
DCB/DCU: [#2021 Data Cache Tag parity error
DCB/DCU: [#2031 Parity error in remote validate RAMs:
DCB/DCU: Port B, Side 0          Bits <23..16>
DCB/DCU: Port B, Side 1          Bits <23..16>
DCB/DCU: Port E, Side 0          Bits <23..16>
DCB/DCU: Port E, Side 1          Bits <23..16>

IPB/IPP: hard_err is not set
VCB/VPC: hard_err is not set
VCB/VPC: softerr is not set
VDB/VPD: hard_err is not set

Register dump for cpu: 1
a0: 000000c8  s0: 00000000 00000000  t0: 00000000   pc:  00000000
a1: 00000000  s1: 00000000 00000000  t1: 000120d0  psw:  666f0950
a2: 00000000  s2: 00000000 00000000  t2: 00000000  ipc:       04e
a3: 00000000  s3: 00000000 00000000  t3: 00000000  ccr:    680000
a4: 00000000  s4: 00000000 00000000  t4: 00000001  cir:    0  tid: 00
a5: 00000000  s5: 00000000 00000000  t5: 000120d0   vl:  00   vs: 00000000
a6: 00000000  s6: 00000000 00000000  t6: 0ad6bad7 vm_u:  00000000 00000000
a7: 00000000  s7: 00000000 00000000  t7: 0ad4bad5 vm_l:  00000000 00000000
global_int_enab: 00  local_int_enab: ff  int_mode: 00  target_CPU: 0  ION: 0

Test 'cpu4030.t' failed
Elapsed time:   0:00:24
: isc
$$$     error in process diagnostic shell
$$$     illegal command 'isc'
: 'iscn sys
iscn:   revision 5.1 (Mon Apr 27 11:43:51 1992)

Initializing the symbol table for 1000 entries
Initializing pcode space to 4000 locations
Initializing p-machine stack to 1000 locations
Unable to open file 'sys' q
\: q
$$$     error in process diagnostic shell
$$$     illegal command '\q'
: q
(spu)> cd /hw/cputest
```

```
(spu)> pwd




/hw/cputest
(spu)> iscn sys
iscn:    revision 5.1 (Mon Apr 27 11:43:51 1992)

Initializing the symbol table for 1000 entries
Initializing pcode space to 4000 locations
Initializing p-machine stack to 1000 locations
Including sys

Verify flag is now on
Including: /hw/cputest/halt_off

 Log_char returning EOF
Including: /hw/cputest/asp_func

 Log_char returning EOF
Including: /hw/cputest/load

 Log_char returning EOF
Including: /hw/cputest/clock

 Log_char returning EOF
Including: /hw/cputest/hard


Display hard error state of cpu with hard (head #)
Default Head [:900]:

 Log_char returning EOF
Including: /hw/cputest/tipr

 Log_char returning EOF
Default Head 1

Before Executing load (addr), TYPE !sysreset

 Log_char returning EOF
iscn68==>!sysreset
sysreset:    revision 5.1 (Mon Apr 27 11:43:53 1992)

 Hit <CR> to continue

iscn68==>!sysreset -12
sysreset:    revision 5.1 (Mon Apr 27 11:43:53 1992)

 Hit <CR> to continue

iscn68==>!cpureg

Register dump for cpu: 1
a0: 000000c8  s0: 00000000 00000000  t0: 00000000   pc:   00000000
a1: 00000000  s1: 00000000 00000000  t1: 00000000  psw:   666f0950
a2: 00000000  s2: 00000000 00000000  t2: 00000000  ipc:       000
a3: 00000000  s3: 00000000 00000000  t3: 00000000  ccr:    680000
a4: 00000000  s4: 00000000 00000000  t4: 00000001  cir:    0  tid: 00
a5: 00000000  s5: 00000000 00000000  t5: 000120d0   vl:   00   vs: 00000000
a6: 00000000  s6: 00000000 00000000  t6: 0ad6bad7 vm_u:   00000000 00000000
a7: 00000000  s7: 00000000 00000000  t7: 0ad4bad5 vm_l:   00000000 00000000
global_int_enab: 00  local_int_enab: ff  int_mode: 00  target_CPU: 0  ION: 0

 Hit <CR> to continue

iscn68==>load 120d0   START TO GO COLDSTART TICK BY TICK
pc = 120d0
iscn68==>tipr
 80
iscn68==>t
pc=00000000   ipc=080   ep=000   ui=f   head 1
iscn68==>t
pc=00000000   ipc=080   ep=000   ui=f   head 1
iscn68==>t
pc=00000000   ipc=080   ep=000   ui=f   head 1
iscn68==>!sysreset
sysreset:    revision 5.1 (Mon Apr 27 11:43:53 1992)

 Hit <CR> to continue

iscn68==>load 120d0
```

```
pc = 120d0




iscn68==>t
pc=00000000    ipc=040    ep=000    ui=f    head 1
iscn68==>t
pc=00000000    ipc=04e    ep=000    ui=f    head 1
iscn68==>t
pc=00000000    ipc=04f    ep=000    ui=f    head 1
iscn68==>t
pc=00000000    ipc=050    ep=000    ui=f    head 1
iscn68==>t
pc=00000000    ipc=051    ep=000    ui=f    head 1
iscn68==>t 5
pc=00000000    ipc=08c    ep=000    ui=f    head 1
iscn68==>tipr
 6a
iscn68==>t
pc=00000000    ipc=06b    ep=000    ui=f    head 1
iscn68==>t
pc=00000000    ipc=06c    ep=000    ui=f    head 1
iscn68==>t
pc=00000000    ipc=06d    ep=000    ui=f    head 1
iscn68==>t
pc=00000000    ipc=06e    ep=000    ui=f    head 1
iscn68==>t
pc=00000000    ipc=070    ep=000    ui=f    head 1
iscn68==>t
pc=00000000    ipc=071    ep=000    ui=f    head 1
iscn68==>t
pc=000120d0    ipc=c00    ep=000    ui=0    head 1
iscn68==>!cpureg

Register dump for cpu: 1
a0: 00000037  s0: 00000000 00000000  t0: 003ffff8  pc:  000120d0
a1: 00000000  s1: 00000000 00000000  t1: 003fe000  psw: 400e00c0
a2: 00000000  s2: 00000000 00000000  t2: 00000ff8  ipc:      c00
a3: 00000000  s3: 00000000 00000000  t3: 00000000  ccr:   600000
a4: 00000000  s4: 00000000 00000000  t4: 0000001b  cir:   0  tid: 00
a5: 00000000  s5: 00000000 00000000  t5: 000120d0   vl:  00   vs: 00000000
a6: 00000000  s6: 00000000 00000000  t6: 0ad6bad7 vm_u: 00000000 00000000
a7: 00000000  s7: 00000000 00000000  t7: 0ad4bad5 vm_l: 00000000 00000000
global_int_enab: 00  local_int_enab: ff  int_mode: 00  target_CPU: 0  ION: 0

 Hit <CR> to continue

iscn68==>t
pc=000120d0    ipc=c00    ep=000    ui=0    head 1
iscn68==>t
pc=000120d0    ipc=c00    ep=000    ui=0    head 1
iscn68==>t
pc=000120d0    ipc=011    ep=000    ui=f    head 1
iscn68==>t
pc=000120d0    ipc=110    ep=000    ui=f    head 1
iscn68==>t
pc=000120d0    ipc=111    ep=000    ui=f    head 1
iscn68==>t
pc=000120d0    ipc=111    ep=000    ui=f    head 1
iscn68==>t
pc=000120d0    ipc=112    ep=000    ui=f    head 1
iscn68==>t
pc=000120d0    ipc=112    ep=000    ui=f    head 1
iscn68==>t
pc=000120d0    ipc=112    ep=000    ui=f    head 1
iscn68==>t
pc=000120d0    ipc=129    ep=000    ui=f    head 1
iscn68==>t
pc=000120d0    ipc=12a    ep=000    ui=f    head 1
iscn68==>t
pc=000120d0    ipc=12b    ep=000    ui=f    head 1
iscn68==>t
pc=000120d0    ipc=011    ep=000    ui=0    head 1
iscn68==>t
pc=000120d0    ipc=c00    ep=000    ui=0    head 1
iscn68==>!sysreset
```

- Next to pc: 000120d0 in the register dump: "wygląda na OK"
- Next to psw: 400e00c0: "? coś tu źle"
- Next to ipc: c00: "← tutaj też bfd"
- Next to the first ipc=011 line: "PTE MISS"
- Next to the repeated ipc=111 and ipc=112 lines: "?"
- Between the last ipc=112 line and the ipc=129 line: "? pewnie był 113, 114"
- Next to the lines from ipc=129 down to the second ipc=011: "ERROR WYKONANIA LOOK IN DEBUGER USZKODZONA PŁYTKA DC translator kodu."

JEŻELI STAJE NA T Podtesicie i ipc≠bfd oznacza, że operacja PTE MISS tworzenia adresu fizycznego do pamięci nie wykonała się prawidłowo. coldstart [illegible] mógł przejść, ·

```
          Subtest 101   CPU:Ø   Ø:ØØ:Ø1    passed
                        CPU:1   Ø:ØØ:ØØ    passed
          Subtest 102   CPU:Ø   Ø:ØØ:Ø1    passed
                        CPU:1   Ø:ØØ:ØØ    passed
          Subtest 103   CPU:Ø   Ø:ØØ:Ø1    passed
                        CPU:1   Ø:ØØ:ØØ    passed
          Subtest 104   CPU:Ø   Ø:ØØ:Ø1    passed
                        CPU:1   Ø:ØØ:ØØ    passed
          Subtest 105   CPU:Ø   Ø:ØØ:Ø1    passed
                        CPU:1   Ø:ØØ:ØØ    passed
          Subtest 110   CPU:Ø   Ø:ØØ:Ø1    passed
                        CPU:1   Ø:ØØ:Ø1    passed
          Subtest 111   CPU:Ø   Ø:ØØ:Ø1    passed
                        CPU:1   Ø:ØØ:ØØ    passed
          Subtest 115   CPU:Ø   Ø:ØØ:Ø1    passed
                        CPU:1   Ø:ØØ:ØØ    passed
          Subtest 116   CPU:Ø   Ø:ØØ:Ø1    passed
                        CPU:1   Ø:ØØ:ØØ    passed
          Subtest 125   CPU:Ø   Ø:ØØ:Ø2    passed
                        CPU:1   Ø:ØØ:ØØ    passed
          Subtest 126   CPU:Ø   Ø:ØØ:Ø1    passed
                        CPU:1   Ø:ØØ:ØØ    passed
          Subtest 130   CPU:Ø   Ø:ØØ:Ø1    passed
                        CPU:1   Ø:ØØ:ØØ    passed
          Subtest 131   CPU:Ø   Ø:ØØ:Ø1    passed
                        CPU:1   Ø:ØØ:ØØ    passed
          Subtest 133   CPU:Ø   Ø:ØØ:Ø1    passed
                        CPU:1   Ø:ØØ:ØØ    passed
          Subtest 132   CPU:Ø   Ø:ØØ:Ø1    passed
                        CPU:1   Ø:ØØ:ØØ    passed
          Subtest 140   CPU:Ø   Ø:ØØ:Ø1    passed
                        CPU:1   Ø:ØØ:ØØ    passed
          Subtest 142   CPU:Ø   Ø:ØØ:Ø1    passed
                        CPU:1   Ø:ØØ:ØØ    passed
          Subtest 144   CPU:Ø   Ø:ØØ:Ø1    passed
                        CPU:1   Ø:ØØ:ØØ    passed
          Subtest 146   CPU:Ø   Ø:ØØ:Ø1    passed
                        CPU:1   Ø:ØØ:ØØ    passed
          Subtest 148   CPU:Ø   Ø:ØØ:Ø2    passed
                        CPU:1   Ø:ØØ:ØØ    passed
          Subtest 150   CPU:Ø   Ø:ØØ:Ø1    passed
                        CPU:1   Ø:ØØ:ØØ    passed
          Subtest 152   CPU:Ø   Ø:ØØ:Ø1    passed
                        CPU:1   Ø:ØØ:ØØ    passed
          Subtest 154   CPU:Ø   Ø:ØØ:Ø1    passed
                        CPU:1   Ø:ØØ:Ø1    passed
          Subtest 200   CPU:Ø   Ø:ØØ:Ø1    passed
                        CPU:1   Ø:ØØ:ØØ    passed
          Subtest 201   CPU:Ø   Ø:ØØ:Ø1    passed
                        CPU:1   Ø:ØØ:ØØ    passed
          Subtest 202   CPU:Ø   Ø:ØØ:Ø1    passed
                        CPU:1   Ø:ØØ:ØØ    passed
          Subtest 205   CPU:Ø   Ø:ØØ:Ø1    passed
                        CPU:1   Ø:ØØ:ØØ    passed
          Subtest 206   CPU:Ø   Ø:ØØ:Ø1    passed
^C  Ø:ØØ:Ø4

^C MENU

Enter:  Ø  to continue test
        1  to abort test
        2  to abort subtest
        3  to abort and pause at end of current subtest
> 1

Test 'cpu4Ø3Ø.t' aborted
```

```
: q
Hit any character to continue('q' to stop):

 Hit <CR> to continue

iscn68==>!sysreset
sysreset:   revision 5.1 (Mon Apr 27 11:43:53 1992)

 Hit <CR> to continue

iscn68==>cpureg

        on line: 29 of file: stdin
 Error token parsed in SESSION
iscn68==>!cpureg

Register dump for cpu: 0
a0: 001a70ac  s0: 00000000 000000a0  t0: 003fff8   pc:  00000000
a1: 00000000  s1: 00000000 0000a0a1  t1: 003fe000  psw: 008000c0
a2: 54555657  s2: 00000000 00005253  t2: 00000ff8  ipc:      000
a3: a4a5a6a7  s3: 00000000 0000a2a3  t3: 23fe85e0  ccr:   000000
a4: a8a9aaab  s4: 00000000 0000a6a7  t4: 00000019  cir:   0  tid: 00
a5: 58595a5b  s5: 00000000 00005657  t5: 00018d10  vl:  00   vs: 00000000
a6: a0a1a2a3  s6: 00000000 0000a0a1  t6: 0ad6bad7 vm_u: 00000000 00000000
a7: 50515253  s7: 00000000 00005051  t7: 0ad4bad5 vm_l: 00000000 00000000
global_int_enab: 00  local_int_enab: ff  int_mode: 00  target_CPU: 0  ION: 0

Register dump for cpu: 1
a0: 00000000  s0: ffffffff ffffffff  t0: 00000000  pc:  00000000
a1: 00000000  s1: ffffffff ffffffff  t1: 00018d10  psw: 800000c0
a2: 00000000  s2: ffffffff ffffffff  t2: 00000000  ipc:      000
a3: ffffffff  s3: ffffffff ffffffff  t3: ffffffff  ccr:   000000
a4: ffffffff  s4: ffffffff ffffffff  t4: 0000001b  cir:   0  tid: 00
a5: ffffffff  s5: ffffffff ffffffff  t5: 00018b80  vl:  00   vs: 00000000
a6: 00000000  s6: ffffffff ffffffff  t6: 0ad6bad7 vm_u: 00000000 00000000
a7: ffffffff  s7: ffffffff ffffffff  t7: 0ad4bad5 vm_l: 00000000 00000000
global_int_enab: 00  local_int_enab: ff  int_mode: 00  target_CPU: 0  ION: 0

 Hit <CR> to continue

iscn68==>!cpureg -i 0

Register dump for cpu: 0
a0: 00000000  s0: 00000000 00000000  t0: 00000000  pc:  00000000
a1: 00000000  s1: 00000000 00000000  t1: 00000000  psw: 008000c0
a2: 00000000  s2: 00000000 00000000  t2: 00000000  ipc:      000
a3: 00000000  s3: 00000000 00000000  t3: 00000000  ccr:   000000
a4: 00000000  s4: 00000000 00000000  t4: 00000000  cir:   0  tid: 00
a5: 00000000  s5: 00000000 00000000  t5: 00000000  vl:  00   vs: 00000000
a6: 00000000  s6: 00000000 00000000  t6: 00000000 vm_u: 00000000 00000000
a7: 00000000  s7: 00000000 00000000  t7: 00000000 vm_l: 00000000 00000000
global_int_enab: 00  local_int_enab: ff  int_mode: 00  target_CPU: 0  ION: 0

Register dump for cpu: 1
a0: 00000000  s0: 00000000 00000000  t0: 00000000  pc:  00000000
a1: 00000000  s1: 00000000 00000000  t1: 00000000  psw: 800000c0
a2: 00000000  s2: 00000000 00000000  t2: 00000000  ipc:      000
a3: 00000000  s3: 00000000 00000000  t3: 00000000  ccr:   000000
a4: 00000000  s4: 00000000 00000000  t4: 00000000  cir:   0  tid: 00
a5: 00000000  s5: 00000000 00000000  t5: 00000000  vl:  00   vs: 00000000
a6: 00000000  s6: 00000000 00000000  t6: 00000000 vm_u: 00000000 00000000
a7: 00000000  s7: 00000000 00000000  t7: 00000000 vm_l: 00000000 00000000
global_int_enab: 00  local_int_enab: ff  int_mode: 00  target_CPU: 0  ION: 0

 Hit <CR> to continue
```

bo ZT5 (NA AS) wychodzi inform. bezpośrednio do PC w IP board czyli jak widać to informacja nie dociera => ale testy przechodzą?
-> uszkodzenie w backplane stykówka
-> inne uszkodzenie

& czasem tak jest, że testy przechodzą sugerując że wszystko ok ale znając kody iscn wiemy, że tak nie jest, nie wykonuje się typu sesji coldstart co tłumaczy także stworzonych pętli dalszych ok

pewnie było 600000

ale PC zera to źle

PC musi = t5 jeśli zakładając się coldstart jeśli nie to może być wówczas tylko iscn

6f0

widać że w procesorze coś się dzieje można zapisać i odczytać widać zmiany a PC – same zera! coś nie tak.

są robaki

zerowanie rejestrów procesora

all zero

iscnoo==>:dshell

c diagnostyka

CONVEX DIAGNOSTIC SHELL

: test cpu4030
cpu4030.t: unable to deterermine software revision

Przy bootowaniu tutaj otrzymaliśmy komunikat o błędzie
Ebusu lub w mm_ ....

Po zrobieniu ~~dump-fest~~ cpureg > filename next
spu)'> hwdump-fest hwd.txt

robimy !sysreset
!initall
dshell
: testujemy mesyny.

Błąd EBUSA oznacza kłopoty z procesorem skalarnym, w ogóle
wredykdowiek jest wskazanie na procesor skalarny to zaczynamy od
testu cpu4030 (najlepszy) - okazuje się że przechodzi
-"- ip24000 także
-"- inne testy przechodzą i co potrzebny wówczas po rekomendacji
do iscn hard -> jakie wskazanie tutaj wszędzie powinny być zera
u nas nie ma W ASP mamy pod SRAM_SYND ff czyli w marginie coś źle
so.

```
Test 'cpu4030.t'                          Tue Feb  9 16:23:13 1993

                        ENTER TEST PARAMETERS

          []       Encloses allowed input ranges or values
          ()       Encloses the default value
          ^        Returns to the previous prompt
          :nn      Returns to the prompt # nn
          :        Returns to the first unsatisfied prompt
          :?       Reviews previous entries

 1: Run default switches? [y,n]                          (y) -> n
 2: Cpus to test:  [ab]                                 (ab) -> b
 3: Forced Faulting Enabled? [y,n]                       (n) ->
 4: Sequential Execution? [y,n]                          (n) ->
 5: Timeout Scale Factor? [1-100]                        (1) ->
 6: Dcache enabled? [y,n]                                (y) ->
 7: Segment of Execution? [0-7]                          (0) ->
 8: Chained Execution Mode? [y,n]                        (n) ->
 9: Loop Enabled? [y,n]                                  (n) ->
10: Hard Errors Enabled? [y,n]                           (y) ->
11: Load Cpu Code? [y,n]                                 (y) -> n
12: Soft Memory Errors Enabled? [y,n]                    (y) ->

                    TEST PARAMETER SUMMARY

Run default switches?                                    : n
Cpus to test:                                            : b
Forced Faulting Enabled?                                 : n
Sequential Execution?                                    : n
Timeout Scale Factor?                                    : 1
Dcache enabled?                                          : y
Segment of Execution?                                    : 0
Chained Execution Mode?                                  : n
Loop Enabled?                                            : n
Hard Errors Enabled?                                     : y
Load Cpu Code?                                           : n
Soft Memory Errors Enabled?                              : y

Loading and initializing test ...  0:00:42
          Current Memory Allocation
File No.  Physical  Address Pid File Name                Logical Offset
       1  00200000-00207fff   0 p0r0_4030               00000000
       2  00208000-0023bfff   0 cpu4030.rnn             00012000
       3  0023c000-0023dfff   0 p0rN_4030               20000000
       4  0023e000-0023ffff   0 p0rN_4030               40000000
       5  00240000-00241fff   0 p0rN_4030               60000000
       6  00242000-00243fff   0 p0rN_4030               80000000
       7  00244000-00246fff   0 pccarry_4030           0000f000
       8  00247000-00249fff   0 pccarry_4030           000ff000
       9  0024a000-0024cfff   0 pccarry_4030           00fff000
      10  0024d000-0024ffff   0 pccarry_4030           0ffff000
      11  00250000-00250fff   0 wrapu_4030             1ffff000
      12  00251000-00251fff   0 wrapu_4030             3ffff000
      13  00252000-00252fff   0 wrapu_4030             5ffff000
      14  00253000-00253fff   0 wrapu_4030             7ffff000
      15  00254000-00254fff   0 wrapu_4030             9ffff000
```

```
  16   00255000-00255fff   0  wrapu_4030         bffff000
  17   00256000-00256fff   0  wrapu_4030         dffff000
  18   00257000-00257fff   0  wrapu_4030         fffff000
  19   00258000-00258fff   0  wrapl_4030         a0000000
  20   00259000-00259fff   0  wrapl_4030         c0000000
  21   0025a000-0025afff   0  wrapl_4030         e0000000
  22   0025b000-00262fff   1  p0r0_4030          00000000
  23   00263000-00296fff   1  cpu4030.rnn        00012000
  24   00297000-00298fff   1  p0rN_4030          20000000
  25   00299000-0029afff   1  p0rN_4030          40000000
  26   0029b000-0029cfff   1  p0rN_4030          60000000
  27   0029d000-0029efff   1  p0rN_4030          80000000
  28   0029f000-002a1fff   1  pccarry_4030       0000f000
  29   002a2000-002a4fff   1  pccarry_4030       000ff000
  30   002a5000-002a7fff   1  pccarry_4030       00fff000
  31   002a8000-002aafff   1  pccarry_4030       0ffff000
  32   002ab000-002abfff   1  wrapu_4030         1ffff000
  33   002ac000-002acfff   1  wrapu_4030         3ffff000
  34   002ad000-002adfff   1  wrapu_4030         5ffff000
  35   002ae000-002aefff   1  wrapu_4030         7ffff000
  36   002af000-002affff   1  wrapu_4030         9ffff000
  37   002b0000-002b0fff   1  wrapu_4030         bffff000
  38   002b1000-002b1fff   1  wrapu_4030         dffff000
  39   002b2000-002b2fff   1  wrapu_4030         fffff000
  40   002b3000-002b3fff   1  wrapl_4030         a0000000
  41   002b4000-002b4fff   1  wrapl_4030         c0000000
  42   002b5000-002b5fff   1  wrapl_4030         e0000000
 ----  23fd6000-23fe9fff   1  pte2               NA
 ----  23fea000-23feafff   1  pte1               NA
 ----  23feb000-23ffefff   0  pte2               NA
 ----  23fff000-23ffffff   0  pte1               NA
      Subtest   1     0:00:01    passed
      Subtest   2     0:00:01    passed
      Subtest   5     0:00:01    passed
      Subtest   6     0:00:01    passed
      Subtest   7     0:00:01    passed
      Subtest  10     0:00:00    passed
      Subtest  11     0:00:01    passed
      Subtest  14     0:00:01    passed
      Subtest  15     0:00:01    passed
      Subtest  16     0:00:01    passed
      Subtest  18     0:00:01    passed
      Subtest  19     0:00:01    passed
      Subtest  20       0:00:03

^C MENU

Enter:  0  to continue test
        1  to abort test
        2  to abort subtest
        3  to abort and pause at end of current subtest
> 1

Test 'cpu4030.t' aborted
: q

 Hit <CR> to continue

iscn68==>!cpureg -c 1

Register dump for cpu: 1
a0: 00000000  s0: 00000000 00000000  t0: 00000000   pc:  00000000
a1: 00000000  s1: 00000000 00000000  t1: 000127b0  psw:  800000c0
a2: 00000000  s2: 00000000 00000000  t2: 00000000  ipc:       000
a3: 00000000  s3: 00000000 00000000  t3: 00000000  ccr:    680000
a4: 00000000  s4: 00000000 00000000  t4: 0000001b  cir:    0  tid: 00
```

inicjalizacja PC po
Z BUSIE Z AS T5 do PC w IP.

np. czyli adres wybrany przez PTE może nie jest adresem fizycznym są zmienione

dalej źle
← bo T5 adres

```
a5: 00000000  s5: 00000000 00000000  t5: 000127e0   v1:  00   vs: 00000000
a6: 00000000  s6: 00000000 00000000  t6: 0ad6bad7 vm_u:  00000000 00000000
a7: 00000000  s7: 00000000 00000000  t7: 0ad4bad5 vm_l:  00000000 00000000
global_int_enab: 00  local_int_enab: ff  int_mode: 00  target_CPU: 0  ION: 0

 Hit <CR> to continue

iscn68==>!mm
mm:   revision 5.1 (Mon Apr 27 11:43:52 1992)
mm:address mode = PHYSICAL
mm(00,00):s log
                    Current sdrs:

sdr[0]=23fffe10 sdr[1]=23fffc10 sdr[2]=23fffa10 sdr[3]=23fff810
sdr[4]=23fff610 sdr[5]=23fff410 sdr[6]=23fff210 sdr[7]=23fff010
mm(00,00):i 120d0,15
0x000120d0       ld.w     #0x55555555,a1
0x000120d6       ld.w     #0xaaaaaaaa,a2
0x000120dc       ld.w     #0xffff,a3
0x000120e0       ld.w     #0xeeeeeeee,a4
0x000120e6       ld.w     #0x77777777,a5
0x000120ec       ld.w     #0x99999999,a6
0x000120f2       ld.w     #0x66666666,a7
0x000120f8       ld.w     #0xaaaaaaaa,a1
0x000120fe       ld.w     #0x55555555,a2
0x00012104       ld.w     #0x0,a3
0x00012106       ld.w     #0x11111111,a4
0x0001210c       ld.w     #0x88888888,a5
0x00012112       ld.w     #0x66666666,a6
0x00012118       ld.w     #0x99999999,a7
0x0001211e       ld.h     #0x0,a1
0x00012120       ld.h     #0x1,a2
0x00012122       ld.h     #0x2,a3
0x00012124       ld.h     #0x3,a4
0x00012126       ld.h     #0x4,a5
0x00012128       ld.h     #0x5,a6
0x0001212a       ld.h     #0x6,a7
mm(00,00):q

 Hit <CR> to continue

iscn68==>in "sys"

Including: sys

Verify flag is now on
Including: /hw/cputest/halt_off

 Log_char returning EOF
Including: /hw/cputest/asp_func

 Log_char returning EOF
Including: /hw/cputest/load

 Log_char returning EOF
Including: /hw/cputest/clock

 Log_char returning EOF
Including: /hw/cputest/hard



Display hard error state of cpu with hard (head #)
Default Head [:900]:

 Log_char returning EOF
```

```
Including: /hw/cputest/tipr

 Log_char returning EOF
Default Head 1

Before Executing load (addr), TYPE !sysreset

 Log_char returning EOF

iscn68==>!sysreset
sysreset:   revision 5.1 (Mon Apr 27 11:43:53 1992)

 Hit <CR> to continue

iscn68==>!cop
cop:   revision 5.1 (Mon Apr 27 11:43:51 1992)

CONVEX Computer Class: 4   Serial Number: 16393
                                                    Revision
Slot    Type    Part Number        Serial No.    Ring  Wire Asm

vda     vpd     410-001206-200     0000560433      1     c    l
vca     vpc     410-002205-200     0000550162      1     c    g
dca     edc     410-001219-200     0000700107      1     b    g
fua     efu     410-001220-200     0000710047      1     a    k
ipa     ipp     410-001207-200     0000570384      1     b    m
asa     asp     410-001209-200     0000590441      1     b    m
vdb     vpd     410-001206-200     0000560438      1     c    l
vcb     vpc     410-002205-200     0000550693      1     c    h
dcb     edc     410-001219-200     0000700087      1     a    g
fub     efu     410-002220-200     0000710134      1     b    j
ipb     ipp     410-001207-200     0000570355      1     b    m
asb     asp     410-001209-200     0000590433      1     b    m
vdc     NONE    000-000000-000     0000000000
vcc     NONE    000-000000-000     0000000000
dcc     NONE    000-000000-000     0000000000
fuc     cxm     410-001181-200     0000790006      1     a    a
ipc     NONE    000-000000-000     0000000000
asc     NONE    000-000000-000     0000000000
vdd     NONE    000-000000-000     0000000000
vcd     NONE    000-000000-000     0000000000
dcd     NONE    000-000000-000     0000000000
fud     cxm     410-001181-200     0000790007      1     a    a
ipd     NONE    000-000000-000     0000000000
asd     NONE    000-000000-000     0000000000
mo0     mcm     410-003213-200     0000530958      2     d    c
me0     mcm     410-003213-200     0001017911      2     e    e
mo1     mcm     410-003213-200     0000530933      2     d    c
me1     mcm     410-003213-200     0000530955      2     d    c
mo2     NONE    000-000000-000     0000000000
me2     NONE    000-000000-000     0000000000
mo3     NONE    000-000000-000     0000000000
me3     NONE    000-000000-000     0000000000
sp4     sp4     410-001223-200     0000660109      1     b    d
cue     cue     410-001222-200     0000740025      1     a    c
cuo     cuo     410-001221-200     0000730004      1     a    e
piy     pi2     410-001224-200     0000720028      2     a    e
pix     NONE    000-000000-000     0000000000
ccu0    iop     410-002218-200     0001010001      1     d    b
ccu1    viop    410-002149-200     0000270515      1     b    k
ccu2    idc     410-001228-200     0000800087      1     b    g
ccu3    NONE    000-000000-000     0000000000
ccu4    NONE    000-000000-000     0000000000
ccu5    NONE    000-000000-000     0000000000
ccu6    NONE    000-000000-000     0000000000
ccu7    NONE    000-000000-000     0000000000
```

```
 Hit <CR> to continue

iscn68==>!sysreset
sysreset:   revision 5.1 (Mon Apr 27 11:43:53 1992)

 Hit <CR> to continue

iscn68==>!cpureg -c 1 -i 0

Register dump for cpu: 1
a0: 00000000  s0: 00000000 00000000  t0: 00000000   pc:  00000000
a1: 00000000  s1: 00000000 00000000  t1: 00000000  psw:  800000c0
a2: 00000000  s2: 00000000 00000000  t2: 00000000  ipc:       000
a3: 00000000  s3: 00000000 00000000  t3: 00000000  ccr:    000000
a4: 00000000  s4: 00000000 00000000  t4: 00000000  cir:    0  tid: 00
a5: 00000000  s5: 00000000 00000000  t5: 00000000   vl:   00   vs: 00000000
a6: 00000000  s6: 00000000 00000000  t6: 00000000 vm_u:  00000000 00000000
a7: 00000000  s7: 00000000 00000000  t7: 00000000 vm_l:  00000000 00000000
global_int_enab: 00  local_int_enab: ff  int_mode: 00  target_CPU: 0  ION: 0

 Hit <CR> to continue

iscn68==>load 120d0
pc = 120d0
iscn68==>t
pc=00000000  ipc=040   ep=000   ui=f   head 1
iscn68==>!cpureg -c 1

Register dump for cpu: 1
a0: 00000000  s0: 00000000 00000000  t0: 00000000   pc:  00000000
a1: 00000000  s1: 00000000 00000000  t1: 000120d0  psw:  800000c0
a2: 00000000  s2: 00000000 00000000  t2: 00000000  ipc:       040
a3: 00000000  s3: 00000000 00000000  t3: 00000000  ccr:    680040
a4: 00000000  s4: 00000000 00000000  t4: 00000000  cir:    0  tid: 00
a5: 00000000  s5: 00000000 00000000  t5: 00000000   vl:   00   vs: 00000000
a6: 00000000  s6: 00000000 00000000  t6: 00000000 vm_u:  00000000 00000000
a7: 00000000  s7: 00000000 00000000  t7: 00000000 vm_l:  00000000 00000000
global_int_enab: 00  local_int_enab: ff  int_mode: 00  target_CPU: 0  ION: 0

 Hit <CR> to continue

iscn68==>t
pc=00000000  ipc=04e   ep=000   ui=f   head 1
iscn68==>!cpureg -c 1

Register dump for cpu: 1
a0: 00000000  s0: 00000000 00000000  t0: 00000000   pc:  00000000
a1: 00000000  s1: 00000000 00000000  t1: 000120d0  psw:  800000c0
a2: 00000000  s2: 00000000 00000000  t2: 00000000  ipc:       04e
a3: 00000000  s3: 00000000 00000000  t3: 00000000  ccr:    680040
a4: 00000000  s4: 00000000 00000000  t4: 00000000  cir:    0  tid: 00
a5: 00000000  s5: 00000000 00000000  t5: 000120d0   vl:   00   vs: 00000000
a6: 00000000  s6: 00000000 00000000  t6: 00000000 vm_u:  00000000 00000000
a7: 00000000  s7: 00000000 00000000  t7: 00000000 vm_l:  00000000 00000000
global_int_enab: 00  local_int_enab: ff  int_mode: 00  target_CPU: 0  ION: 0

 Hit <CR> to continue

iscn68==>tipr
 80
iscn68==>t 5
pc=00000000   ipc=080   ep=000   ui=f   head 1
iscn68==>t
pc=00000000   ipc=081   ep=000   ui=f   head 1
iscn68==>t
```

```
pc=00000000   ipc=068   ep=000   ui=f   head 1
iscn68==>t
pc=00000000   ipc=069   ep=000   ui=f   head 1
iscn68==>t
pc=00000000   ipc=06a   ep=000   ui=f   head 1
iscn68==>t
pc=00000000   ipc=06b   ep=000   ui=f   head 1
iscn68==>t
pc=00000000   ipc=06c   ep=000   ui=f   head 1
iscn68==>t
pc=00000000   ipc=06d   ep=000   ui=f   head 1
iscn68==>t
pc=00000000   ipc=06e   ep=000   ui=f   head 1
iscn68==>t
pc=00000000   ipc=070   ep=000   ui=f   head 1
iscn68==>t
pc=00000000   ipc=071   ep=000   ui=f   head 1
iscn68==>t
pc=00000000   ipc=c00   ep=000   ui=0   head 1
iscn68==>t
pc=00000000   ipc=c00   ep=000   ui=0   head 1
iscn68==>!cpureg -c 1

Register dump for cpu: 1
a0: 00000000  s0: 00000000 00000000  t0: 003ffff8   pc:   00000000
a1: 00000000  s1: 00000000 00000000  t1: 003fe000  psw:   000000c0
a2: 00000000  s2: 00000000 00000000  t2: 00000ff8  ipc:        c00
a3: 00000000  s3: 00000000 00000000  t3: 00000000  ccr:     600000
a4: 00000000  s4: 00000000 00000000  t4: 0000001b  cir:    0   tid: 00
a5: 00000000  s5: 00000000 00000000  t5: 000120d0   vl:   00    vs: 00000000
a6: 00000000  s6: 00000000 00000000  t6: 0ad6bad7 vm_u:   00000000 00000000
a7: 00000000  s7: 00000000 00000000  t7: 0ad4bad5 vm_l:   00000000 00000000
global_int_enab: 00   local_int_enab: ff   int_mode: 00   target_CPU: 0   ION: 0

 Hit <CR> to continue

iscn68==>t
pc=00000000   ipc=c00   ep=000   ui=0   head 1
iscn68==>t
pc=00000000   ipc=011   ep=000   ui=f   head 1
```

ostatnie instr. w op. code

źle

Reanalyze kodu 0 oznacza że połączenie AS z APP źle

071483

#908 [illegible]
2U Func Unit 2 [illegible]
DC - [illegible] C
DB - [illegible] B
DD - [illegible] D.

cocyt021

Test 'cpu4233.t'   Mon Feb 8 09:13:10 1993

ENTER TEST PARAMETERS

[] Encloses allowed input ranges or values
() Encloses the default value

```
         ^        Returns to the previous prompt
         :nn      Returns to the prompt # nn
         :        Returns to the first unsatisfied prompt
         :?       Reviews previous entries

 1: Run default switches? [y,n]                          (y) ->

                  TEST PARAMETER SUMMARY

Run default switches?                                      : y

Loading and initializing test ...  0:01:27
        Current Memory Allocation
File No.  Physical  Address Pid File Name                  Logical Offset
       1  00200000-0023ffff   0 p0r0_4233                 00000000
       2  00240000-002a4fff   0 cpu4233.rnn               00027000
       3  002a5000-00aa4fff   0 support_4233              e0000000
    ----  23ff8000-23ff9fff   0 pte2                       NA
    ----  23ffa000-23ffdfff   0 ptet                       NA
    ----  23ffe000-23ffefff   0 pte2                       NA
    ----  23fffc00-23ffffff   0 pte1                       NA
        Subtest 500    0:00:02   failed

*****  Mon Feb  8 09:15:29 1993  *****
Test:     cpu4233.t  1.30   Class: 12   Subtest: 500 1.25  Count: 1    Error: 0
Failed:  remote invalidate 1, single head writing bytes, other heads spin on cmr
HARD ERROR DETECTED
hard_logger:   revision 5.1 (Mon Apr 27 11:43:51 1992)
Data Cache
Left parity bit => Left data byte, Left validity bit => Left data byte.
ADDR  DATA      P TAG_A  P TAG_BC P TAG_DE P  VBS  VCS  VDS  VES  UPD
0008  00000000 f 0ad6b0 4 0ad6bc 4 0ad6bc 4  0 0  0 0  0 0  0 0  00
ODD   00000000 f 0ad6b0 4 7f0010 4 9f0004 4  0 0  0 0  0 0  0 0  00
0018  00000000 f 0ad6b0 4 0ad6bc 4 0ad6bc 4  0 0  0 0  0 0  0 0  00
ODD   00000000 f 0ad6b0 4 3f0011 0 ff0020 4  0 0  0 0  0 0  0 0  00
ME0/MCM: hard_err is not set
ME0/MCM: soft_err is not set
MO0/MCM: hard_err is not set
MO0/MCM: soft_err is not set
ME1/MCM: hard_err is not set
ME1/MCM: soft_err is not set
MO1/MCM: hard_err is not set
MO1/MCM: soft_err is not set
CU0: hard_err is not set
CUE: hard_err is not set
PIY/PI2: hard_err is not set
PIY/PI2: pia_softerr is not set
RITA:   [#900] EDC detected EFU hard error
RITA:
RITA:    EFU field              CPU: A          B          C          D
RITA:    -------------------    ---------- ---------- ---------- ----------
RITA:    phi0                      0x00000    0x00000
RITA:    phi1                      0x00000    0x00000
RITA:    phi2                      0x3ffff    0x3ffff
RITA:    qpar_err                    0x00       0x18
RITA:    ram_par_err                 0x00       0x38
RITA:    ri_adr_pe                   0x00       0x00
RITA:    even_addr_reg_2[0]         0x200      0x200
RITA:    even_addr_reg_2[1]         0x200      0x200
RITA:    even_addr_reg_2[2]         0x200      0x200
RITA:    odd_addr_reg_2[0]          0x200      0x200
RITA:    odd_addr_reg_2[1]          0x200      0x200
RITA:    odd_addr_reg_2[2]          0x200      0x200
RITA:    ri_data_pe                  0x00       0x00
RITA:    even_data_reg_2[0]         0x1b4      0x1b4
RITA:    even_data_reg_2[1]         0x0d6      0x0d6
```

=> it means OK

wnoświej' by to # 908

```
RITA:    even_data_reg_2[2]          Øx1Øa       Øx1Øa
RITA:    odd_data_reg_2[Ø]           Øx1b4       Øx1b4
RITA:    odd_data_reg_2[1]           ØxØd6       ØxØd6
RITA:    odd_data_reg_2[2]           Øx1Øa       Øx1Øa
RITA:
RITA:    CXM field              CPU: A          B          C          D
RITA:    -------------------    ----------  ---------  ---------  ---------
RITA:    phiØ                                          ØxØØØØØ    ØxØØØØØ
RITA:    phi1                                          ØxØØØØØ    ØxØØØØØ
RITA:    phi2                                          ØxØØØØ1    ØxØØØØ1
RITA:    harderr                                           ØxØ        ØxØ
RITA:    riØ_out                                    ØxØ478ØØØØ ØxØ478ØØØØ
RITA:    riØ_out << 3                               Øx23cØØØØØ Øx23cØØØØØ
RITA:    riØ_pout                                          Øx5        Øx5
RITA:    write_reqØ_out                                    ØxØ        ØxØ
RITA:    riØ_synd                                          ØxØ        ØxØ
RITA:    ri1_out                                    ØxØ478ØØØØ ØxØ478ØØØØ
RITA:    ri1_out << 3                               Øx23cØØØØØ Øx23cØØØØØ
RITA:    ri1_pout                                          Øx5        Øx5
RITA:    write_req1_out                                    ØxØ        ØxØ
RITA:    ri1_synd                                          ØxØ        ØxØ
RITA:    function    out bits              pout    good parity
RITA:    ram data    <31..24>               <3>    ØxØØ -> 1
RITA:    ram data    <23..16>               <2>    ØxØØ -> 1
RITA:    ram data    <15..12>,write_req     <1>    ØxØØ -> Ø
RITA:    ram addr    <11.. 3>               <Ø>    ØxØØ -> 1
RITA:
RITA:    [#9Ø2] EFU[1]:qpar_err is not OR of expected fields
RITA:    [#9Ø4] EFU[1]:ram_par_err: Øx38 (odd[2] odd[1] odd[Ø])
RITA:    z[#9Ø6] RITA tag ram address parity problem probably on or between
RITA:           CPUs C and D
RITA:       RITA tag ram address is <11..3> of the <31..3> address
RITA:       examine EFU ri_adr_pe and CXM riØ_synd, ri1_synd
RITA:    [#9Ø8] RITA tag ram data parity problem probably on or between
RITA:           CPUs C and D
RITA:       RITA tag ram data is <31..12> and write_req of the <31..3> address
RITA:       examine EFU ri_data_pe and CXM riØ_synd, ri1_synd
RITA:    [#91Ø] qpar_err suggests problem probably on or between
RITA:           CPUs B and A

ASA/ASP: hard_err is not set
DCA/EDC: hard_err is not set
IPA/IPP: hard_err is not set
VCA/VPC: hard_err is not set
VCA/VPC: softerr is not set
VDA/VPD: hard_err is not set
ASB/ASP: hard_err is not set
DCB/EDC: Hard error detected.
DCB/EDC: [#2Ø6] EDC detected EFU hard error
DCB/EDC: [#2Ø8] efu parity error in RITA gate array - see previous messages

IPB/IPP: hard_err is not set
VCB/VPC: hard_err is not set
VCB/VPC: softerr is not set
VDB/VPD: hard_err is not set

Test 'cpu4233.t' failed
Elapsed time:   Ø:ØØ:52
```

← Rita czyli niewmieszczenie się na płytkach procesora rys. 6-11 handout

ok (beside the first hard_err group)

błąd albo w backplane or plane connector or którejś z płyt procesora wokół niej tutaj backplane B i C. (wymiana wcześniej może być płytki DC bo one także mogą być celem w tym.

→ płytki w EFU I DC board w CPU B is dead

ok tam coś takiego wypisują